REMARKS

Claims 1-25 and 27-36 were pending in the application. Claims 17 and 35 have been cancelled. Claims 1, 12, 18, 19, 21 and 30 have been amended. Independent claim 1 has been amended to correspond more closely with the features recited in independent claim 21. Accordingly, claims 1-16, 18-25, 27-34, and 36 remain pending subsequent entry of the present amendment.

Claim Objection

Claim 21 has been amended to overcome the objection.

35 U.S.C. § 103 REJECTIONS

In the present Office Action, claims 1-25 and 27-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Obana et al. (U.S. Patent 5,001,711, hereinafter "Obana") in view of Yamato et al. (U.S. Patent 6,041,062 (hereinafter "Yamato"), and in further view of Shibagaki et al. U.S. Patent 4,704,715 (hereinafter "Shibagaki"). Applicant respectfully traverses these rejections and requests reconsideration in view of the following discussion.

Applicant submits that claim 1 recites features that are neither disclosed nor suggested by the cited art. On page 3, paragraph 1 of the present Office Action, the examiner states that Obana discloses "converting the recovered data into at least two intermediate-speed data channels (DS2 signals), wherein each intermediate-speed data channel is timed by a first clock based on the reference clock (Fig. 5 and col. 5, lines 6-54); converting each intermediate-speed data channel into at least two low-speed data channels (DS1 signals), wherein the low-speed data channels in aggregate contain the recovered data and each low-speed data channel is timed by a second clock based on the reference clock (Fig. 5 and col. 5, lines 6-54)." However, Applicant submits that there

are significant differences between the disclosure of Obana and the features of claim 1. For example, claim 1 recites a method which includes:

> "receiving a tributary complying with a jitter tolerance;
> recovering data from the tributary;
> receiving a reference clock;
> **retiming the recovered data according to the reference clock;**
> converting the recovered data into at least two intermediate-speed data channels, wherein **each intermediate-speed data channel is timed by a first clock based on the reference clock;**
> converting each intermediate-speed data channel into at least two low-speed data channels, wherein the low-speed data channels in aggregate contain the recovered data and **each low-speed data channel is timed by a second clock based on the reference clock**;
> modulating each low-speed data channel to generate a corresponding low-speed symbol channel; and
> frequency division multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission in optical form across the communications system." (emphasis added).

Applicant submits all of the above highlighted features of claim 1 are neither disclosed nor suggested by the cited art. Generally speaking, Applicant's claim 1 is concerned with maintaining jitter tolerance. As can be seen from the above, the method comprises multiple steps including the timing of data channels at multiple (three) different speeds. More specifically, data from the tributary is recovered, retimed according to a reference clock, and converted into intermediate-speed data channels that are timed by a first clock based on the reference clock. The intermediate-speed data channels are then converted into low-speed data channels. The low-speed data channels are timed by a second clock based on the reference clock. Thus, there is a reference clock, a first clock, and a second clock. Applicant submits that at least one of these clocks is not disclosed by the cited art.

In contrast to the presently claimed invention, Obana is generally directed to reducing the number of clock pins needed by an apparatus for performing multiplexing/demultiplexing. Obana's apparatus includes its own clock generating unit

that supplies at least some of the required clock signals. More specifically, Obana discloses:

> "The present invention provides complex multiplexer/demultiplexer apparatus which includes:
>
> a plurality of first multiplex means 21 which multiplex input first order group data signals DS1 to convert them into middle order group (second order group) data signals DS2,
>
> a second multiplex means 24 which multiplexes the middle order group (second order group) data signals DS2 to convert them into high order group (third order group) data signals DS3,
>
> a first demultiplex means 25 which demultiplexes the input high order group (third order group) data signals DS3 to convert them into middle order group (second order group) data signals DS2,
>
> a plurality of second demultiplex means 28 which demultiplex the middle order group (second order group) data signals DS2 to convert them into low order group (first order group) data signals DS1, and
>
> a clock generating means 29 which supplies the timing clocks required by the above means, wherein
>
> the second multiplex means 24 operates in synchronization with the basic clock signal CK_B prepared by the clock generating means 29, the first multiplex means 21 operates in synchronization with a second order group data clock which is formed by applying speed conversion to a second order group common clock CK_C formed by frequency dividing the basic clock signal CK_B, the second order group data clock completely bit synchronized with the middle order group common clock CK_C, but the second order group data clock including empty bits which are produced at a fixed cycle and the clock rate of the second order group data clock being lower than the clock rate of the second order group common clock,
>
> the first demultiplex means 25 operates in synchronization with a clock CK_α given from a remote office (or external line), the second demultiplex means 28 operates in synchronization with the second order group data clock formed by applying speed conversion to a clock formed by frequency dividing the basic clock signal extracted from the input second order group data signal, the second order group data clock completely bit synchronized with the second order group common clock CK_C, formed by frequency dividing the basic clock signal, but the second order group data clock including empty bits which are produced at a fixed cycle and the

> clock rate of the second order group data clock being lower than the clock rate of the second order group common clock CK_C." (Obana, col. 5, lines 6-54).

In the following discussion, the multiplexing and demultiplexing means will be considered separately. With respect to the multiplexing means of Obana, it is apparent that the multiplexing means of Obana differs from the recited features of claim 1 in that low-speed (DS1) data signals are combined into intermediate-speed (DS2) signals, which are combined into high-speed (DS3) signals, rather than the recited conversions from a tributary to intermediate-speed and then to low-speed.

In addition to the above, Obana's demultiplexing means differs from the recited features of claim 1 as well. In contrast to the claimed limitations, Obana merely discloses

> "the first demultiplex means 25 operates in synchronization with a clock CK_α given from a remote office (or external line), the second demultiplex means 28 operates in synchronization with the second order group data clock." (Obana, col. 5, lines 40-44).

The second order group data clock is also referred to as "CK_D". Obana describes "CK_D" in the following:

> "Further, the speed converter 33 includes an AI bit extraction unit 65 which extracts the additional information bits AI in the input signals DS2, an AI bit deletion unit 67 which deletes the additional information bits, a stuffing detection unit 66 which detects the stuffing, and a destuffing control unit 68 which performs destuffing control in accordance with the detected stuffing, and a clock generating unit 64 which generates a clock signal (CK_D) including empty bits in accordance with the detected stuffing.
>
> The clock generating unit 64 is supplied with the results of the stuffing detection of the stuffing detection unit 66 and the 6.391 MHz second order group common clock CK_C output from the frequency divider 47 and supplies a 6.312 MHz clock signal including empty bits to the M12 demultiplexer unit 34. (Obana, col.10, lines 10-26 and figure 9A).

As can be seen from the above, the second order group data clock operates at the same bit rate as the second order group data signals, 6.312 MHz, i.e., the bit rate of the DS2 signals modified by the addition of stuff bits. Note also that both the second order group data clock and the second order group data signals are inputs to the second demultiplexer. It is noted that Obana does not disclose that the **outputs** of the second demultiplex means are timed by CK_D nor by any clock whatsoever. Therefore, Applicant submits that a demultiplexer operating "in synchronization with a ... clock" as disclosed by Obana refers to the process by which the demultiplexer distinguishes one channel from another within the input (DS2) signal, an interpretation that is further supported by the fact that the demultiplexer's input signal and clock have the same data rate. Applicant submits that for similar reasons, Obana's first demultiplex means operating in synchronization with "CK_α" refers to distinguishing one channel from another within the input (DS3) signal of the first demultiplex means. However, Obana does not disclose synchronizing the output (DS1) signal of the second demultiplex means to any clock whatsoever.

Accordingly, Applicant finds no teaching or suggestion in Obana of "retiming the recovered data according to the reference clock, converting the recovered data into at least two intermediate-speed data channels, wherein each intermediate-speed data channel is timed by a first clock based on the reference clock, and converting each intermediate-speed data channel into at least two low-speed data channels, wherein the low-speed data channels in aggregate contain the recovered data and each low-speed data channel is timed by a second clock based on the reference clock" as is recited in amended claim 1. Likewise, the features discussed above are wholly absent from Yamato and Shibagaki. Therefore, Applicant submits that claim 1 is patentably distinguishable from the cited art, taken either singly or in combination, for at least the above reasons. As independent claims 21 and 37 include features similar to those of claim 1, claims 21 and 37 are believed patentably distinguishable from the cited art for similar reasons. Likewise, each of dependent claims 2-11, 22-25, and 27-29 are believed patentably distinguishable from the cited art for at least the above reasons as well.

Also, regarding claim 10, in paragraph 15 of the present Office Action, the Examiner states that Obana discloses:

> "aligning the timing for the receive-side low-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); and time division multiplexing the receive-side recovered data from the receive-side low-speed data channels into the at least two receive-side intermediate-speed data channels according to the aligned timing (Obana: col. 5, lines 6-15 and col. 5, lines 26-39) ."

However, Applicant submits that there are significant differences between Obana and the features of claim 10 quoted by the Examiner. The claimed low-speed data channels are aligned, data is recovered from them, and the recovered data is multiplexed into intermediate-speed data channels. Accordingly, aligning the timing takes place on the data channels before they are multiplexed, i.e., on the input side of the multiplexer. In contrast, Obana discloses:

> "The M12 units 30 are each provided with an M12 multiplexer unit 31 which multiplexes four first order group data signals DS1, an M12 demultiplexer unit 34 which demultiplexes signals to obtain four first order group data signals DS1, a speed converter 32 which performs speed conversion on signals by insertion of additional information bits (AI), and a speed converter 33 which performs speed conversion on signals by separation (deletion) of the additional information bits.
>
> The speed converter 32 is supplied with a 6.391 MHz order group common clock CK_C and frame timing pulse FTP (FIG. 11) supplied from the M23 unit 40. The speed converter 32 outputs a signal DS2 converted in speed to 6.391 Mbps by insertion of additional information bits into the second order group signals DS2 output from the M12 multiplexer unit 31 based on the clock signals and frame timing pulses." (Obana, col. 7, lines 41-57)

As can be seen from the above, DS2 signals, **output** from the M12 multiplexer unit, are timed by a 6.391 MHz clock. However, Obana does not disclose aligning the timing of the **inputs** to the M12 multiplexer unit (i.e., DS1 signals).

Accordingly, Applicant finds no teaching or suggestion in Obana of aligning a timing for the receive-side low-speed data channels and time division multiplexing the receive-side recovered data from the receive-side low-speed data channels into the at least two receive-side intermediate-speed data channels according to the aligned timing. Likewise, the features discussed above are wholly absent from Yamato and Shibagaki. Therefore, Applicant submits that claim 10 is patentably distinguishable from the cited art, taken either singly or in combination, for at least the above reasons. Claims 17, 29, and 35 include features similar to those of claim 10. Independent claim 12 has been amended to include the some of the features of claim 10 and all of the features of claim 17. Independent claim 30 has been amended to generally include the features of claim 35. Accordingly, claims 12 as amended, 29, and 30 as amended are believed patentably distinguishable from the cited art for similar reasons. Likewise, claims 11, 13-16, 18-20, 31-34, and 36 include all of the features of the claims upon which they depend and are thus believed patentably distinguishable from the cited art for at least the above reasons as well.

Applicant believes all claims to be in condition for allowance.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5957-41406/RDR.

Respectfully submitted,

Rory D. Rankin
Reg. No. 47,884
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin,
Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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